Claims

What is claimed is:

1. A method for monitoring T-top gate formation comprising:

providing a wafer structure undergoing a T-top gate fabrication process;

generating a signature associated with the wafer structure during a process step to monitor formation of the T-top gate; and

comparing the generated signature to a signature store to determine a state of the T-top gate.

2. The method of claim 1, wherein a scatterometry system is employed to generate the signature associated with the wafer structure.

3. The method of claim 1, wherein generating the signature comprises:

directing a beam of incident light at the wafer structure;

collecting a light reflected from the wafer structure; and

transforming the reflected light into the signature.

4. The method of claim 1, wherein the signature corresponds to a particular profile associated with the wafer undergoing T-top gate formation.

5. The method of claim 1, wherein an analysis system compares the generated signature to the signature store to determine the state of the T-top gate.

6. The method of claim 1, further comprising feeding information relating to the state of the T-top gate back into the T-top gate fabrication process to optimize T-top gate formation.

7. An in-line method for determining T-top gate dimensions comprising:

providing a wafer structure having a T-top gate formed thereon;

generating a signature associated with the T-top gate;

comparing the generated signature with a signature store to determine the dimensions of the T-top gate; and

if the dimensions of the T-top gate are not within a pre-determined acceptable range, then adjusting T-top gate process parameters using feedback control.

8. The method of claim 7, wherein a scatterometry system is employed to generate the signature associated with the T-top gate.

9. The method of claim 7, wherein generating the signature comprises:

directing a beam of incident light at the wafer structure;

collecting a light reflected from the wafer structure; and

transforming the reflected light into the signature.

10. The method of claim 7, wherein the signature corresponds to a particular profile associated with the wafer undergoing T-top gate formation.

11. The method of claim 7, wherein an analysis system compares the generated signature to the signature store to determine the state of the T-top gate.

12. The method of claim 7, wherein adjusting T-top gate process parameters using feedback control comprises feeding information relating to the state of the T-top gate back into the T-top gate fabrication process to optimize T-top gate formation.

13. The method of claim 7, wherein T-top gate dimensions comprises amount of undercut and effective gate width.

14. The method of claim 7, further comprising generating a schematic cross-section of the T-top gate to determine its profile and dimensions.

15. The method of claim 14, wherein the schematic cross-section of the T-top gate is generated from the light reflected from the wafer structure.

16. An in-line method for determining T-top gate dimensions comprising:

providing a wafer structure having a T-top gate formed thereon;

directing an incident beam of light at the T-top gate;

collecting the reflected light associated with the T-top gate;

generating a signature associated with the T-top gate using the reflected light;

comparing the generated signature with a signature store to determine the dimensions of the T-top gate; and

if the dimensions of the T-top gate are not within a pre-determined acceptable range, then adjusting T-top gate process parameters using feedback control.

17. The method of claim 16, wherein a scatterometry system is employed to generate the signature associated with the T-top gate.

18. The method of claim 16, wherein the signature corresponds to a particular profile associated with the wafer undergoing T-top gate formation.

19. The method of claim 16, wherein an analysis system compares the generated signature to the signature store to determine the state of the T-top gate.

20. The method of claim 16, wherein adjusting T-top gate process parameters using feedback control comprises feeding information relating to

the state of the T-top gate back into the T-top gate fabrication process to optimize T-top gate formation.

21. The method of claim 16, wherein T-top gate dimensions comprises amount of undercut and effective gate width.

22. The method of claim 16, further comprising generating a schematic cross-section of the T-top gate to determine its profile and dimensions.

23. The method of claim 22, wherein the schematic cross-section of the T-top gate is generated from the light reflected from the wafer structure.

24. An in-line system for monitoring T-top gate formation comprising:

a wafer structure undergoing a T-top gate formation process;

a T-top gate formation monitoring system for generating a signature associated with wafer surface dimensions during a process step; and

a signature store coupled to the monitoring system, wherein the generated signature is compared to the signature store to determine a state of the T-top gate.

25. The system of claim 24, wherein the T-top gate formation monitoring comprises a scatterometry system.

26. The system of claim 24, wherein the T-top gate formation signature store comprises known signatures of wafer structures as they appear during the T-top gate formation process.

27. The system of claim 24, wherein the signature corresponds to a particular profile associated with the wafer undergoing T-top gate formation.

28. The method of claim 24, wherein wafer surface dimensions comprise

amount of undercut and effective gate width.

29. The method of claim 24, comprising a feedback control system operatively coupled to the T-top gate formation monitoring system.

30. An in-line system for determining T-top gate dimensions comprising:

a wafer structure undergoing a T-top gate formation process;

a scatterometry system coupled to the formation process for directing light at and collecting reflected light from the wafer structure;

a signature store comprising known signatures associated with T-top gate formation;

a T-top gate formation analysis system coupled to the scatterometry system and to the signature store for determining the T-top gate dimensions; and

a feedback control system coupled to the T-top gate formation analysis system for optimizing T-top gate formation.

31. The system of claim 30, wherein the T-top gate formation signature store comprises known signatures of wafer structures as they appear during the T-top gate formation process.

32. The system of claim 30, wherein the signature corresponds to a particular profile associated with the wafer structure undergoing T-top gate formation.

33. The method of claim 30, wherein the T-top gate dimensions comprise amount of undercut and effective gate width.

34. An in-line system for determining T-top gate dimensions comprising:

means for providing a wafer structure having a T-top gate formed thereon;

means for generating a signature associated with the T-top gate;

means for comparing the generated signature with a signature store to determine the dimensions of the T-top gate; and

if the dimensions of the T-top gate are not within a pre-determined acceptable range, then means for adjusting T-top gate process parameters using feedback control.